UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/257,506	02/25/1999	TATSUYA MATSUMURA	50073-019	2315

20277 7590 11/18/2004

MCDERMOTT WILL & EMERY LLP
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

EXAMINER	
NELSON, ALECIA DIANE	
ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/257,506	MATSUMURA ET AL.	
	Examiner	Art Unit	
	Alecia D. Nelson	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4 and 6* is/are allowed.

6)☒ Claim(s) *5 and 7-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. ***Claims 5, 7, and 8*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujisawa et al. (U.S. Patent No. 5,038,139) in view of Jeong et al. (U.S. Patent No. 6,144,242).

With reference to **claims 5, 7, and 8,** Fujisawa et al. teaches a half tone display driving circuit for a liquid crystal matrix panel, wherein due to generated

noise due to simultaneous switching of adjacent column signals is suppressed (see column 1, lines 18-24). The method of which voltages of adjacent column driving signals (19) change to produce rise edge and fall edge at the same timing, respectively, whereby noises induced in row driving signals (21) can be cancelled to eliminate or suppress a decrease in brightness of the display (see column 10, lines 45-55).

Even though Fujisawa et al. identifies the problem of noise generated by the column and row driving signals, which causes a decrease in brightness of the display, there fails to be any teaching that the noise is suppressed by delaying the driving signals.

Jeong et al. teaches electronic and computer technology wherein large amounts of data required for data communications in intensive data consuming systems using graphical or video information, multiple input-output channels, and the like, wherein circuitry for is used for driving signals onto a communication line in order to reduce noise in the signal transmission. Jeong et al. teaches the usage controllable delays, wherein data signals (d0(t)) are digital and are synchronized in that they each may have transitions only at periodic points in time. However instead of the transitions being synchronized, they are slightly out-of-synch with one another. Thereby, each of the controlled intervals of time are significantly less in magnitude and the controlled intervals of time are generally different in length from each other such that the transitions of the various signals are generally slightly out-of-sync (see column 2, lines 45-65).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for delay in the time lengths of the data signals, as taught by Jeong et al, wherein the rate of delay of the data signals are at controlled intervals, to be used in a liquid crystal display system which has a need for the amount of noise generated to be reduced in a system similar to that which is taught by Fujisawa et al. By allowing the usage of the circuitry of Jeong et al. in the LCD of Fujisawa et al. the LCD is capable of displaying high quality images without a decrease in brightness by reducing EMI without significantly impacting on the performance of the liquid crystal display.

3. ***Claims 9-13*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimamoto (U.S. Patent No. 6,147,672) in view of Jeong et al.

With reference to **claims 9-13**, Shimamoto teaches a driving method wherein a display controller (1) outputs digital display signals (6-bit RGB signals) to be displayed on a flat panel display such as a liquid crystal display device (see column 5, lines 46-49), which are transferred from a display timing circuit (17) to a TFT drive circuit (57, 59) for driving a LCD panel (see column 6, lines 32-37).

Even though Shimamoto teaches that it is necessary to slow down the transfer of display data (see column 1, lines 35-49) it is not disclosed the usage of a delay unit provided in the display timing control circuit for delaying the transfer timing between one bit unit and another.

Jeong et al. teaches electronic and computer technology wherein large amounts of data required for data communications in intensive data consuming

systems using graphical or video information, multiple input-output channels, and the like, wherein circuitry for is used for driving signals onto a communication line in order to reduce noise in the signal transmission. Jeong et al. teaches the usage controllable delays, wherein data signals (d0(t)) are digital and are synchronized in that they each may have transitions only at periodic points in time. However instead of the transitions being synchronized, they are slightly out-of-synch with one another. Thereby, each of the controlled intervals of time are significantly less in magnitude and the controlled intervals of time are generally different in length from each other such that the transitions of the various signals are generally slightly out-of-sync (see column 2, lines 45-65).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for delay in the transfer of the data signals, as taught by Jeong et al, to be used in a liquid crystal display system which has a need to slow down the transfer in order for the amount of noise generated to be reduced in a system similar to that which is taught by Shimamoto. Therefore, by allowing the usage of the circuitry of Jeong et al. in the LCD timing controller of Shimamoto, the LCD is capable of displaying high quality color images without a decrease in brightness by reducing EMI, and in doing without significantly impacting on the performance of the liquid crystal display.

Allowable Subject Matter

4. ***Claims 1-4 and 6*** are allowed.

The following is an examiner's statement of reasons for allowance: With reference to **claim 1**, none of the references used either singularly or in combination teach or fairly suggest an internal clock generating circuitry for generating a plurality of internal clock signals sequentially delayed and a data latch circuit for receiving a plurality of display data signals having a respective point of change. The data latch circuit outputs the plurality of display data signals each sequentially delayed in accordance with the plurality of internal clock signals. Newly cited reference Kubota et al. (U.S. Patent No. 6,437,768) teaches a register circuit which includes a clock generating circuit, the data latch circuit, and the delay, however the data latch circuit does not receive the display data signals as claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

5. Applicant's arguments with respect to ***claims 1, 3-5, and 7-13*** have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**.

See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is (703) 305-0143. The examiner can normally be reached on Monday-Friday 9:30-6:00. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-2600.

adn/And
November 13, 2004

AMR A. AWAD
PRIMARY EXAMINER